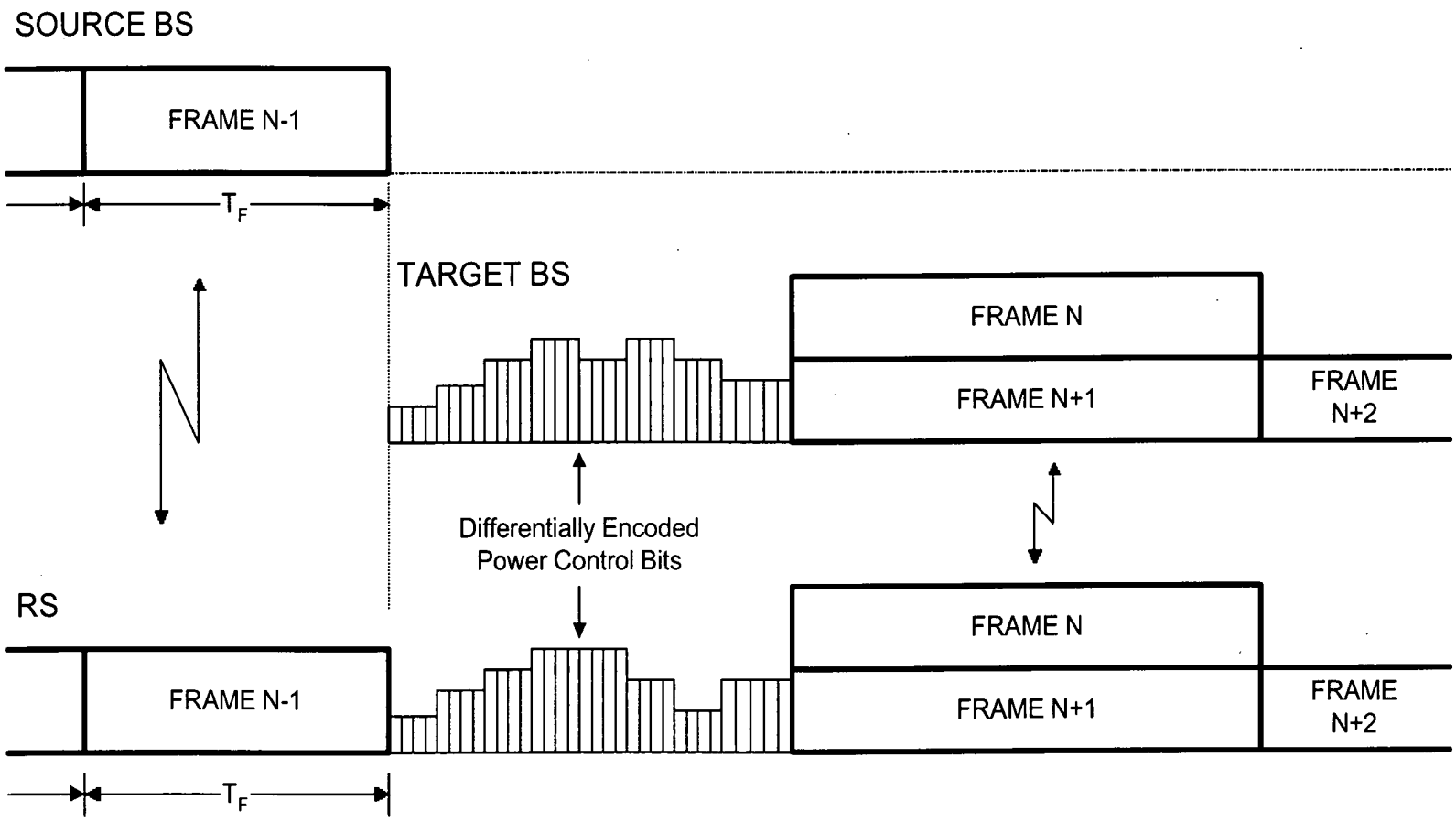

SOURCE BS
FRAME N-1
T_F
TARGET BS
FRAME N
FRAME N+1
FRAME N+2
Differentially Encoded Power Control Bits
RS
FRAME N-1
FRAME N
FRAME N+1
FRAME N+2
T_F

FIG. 25

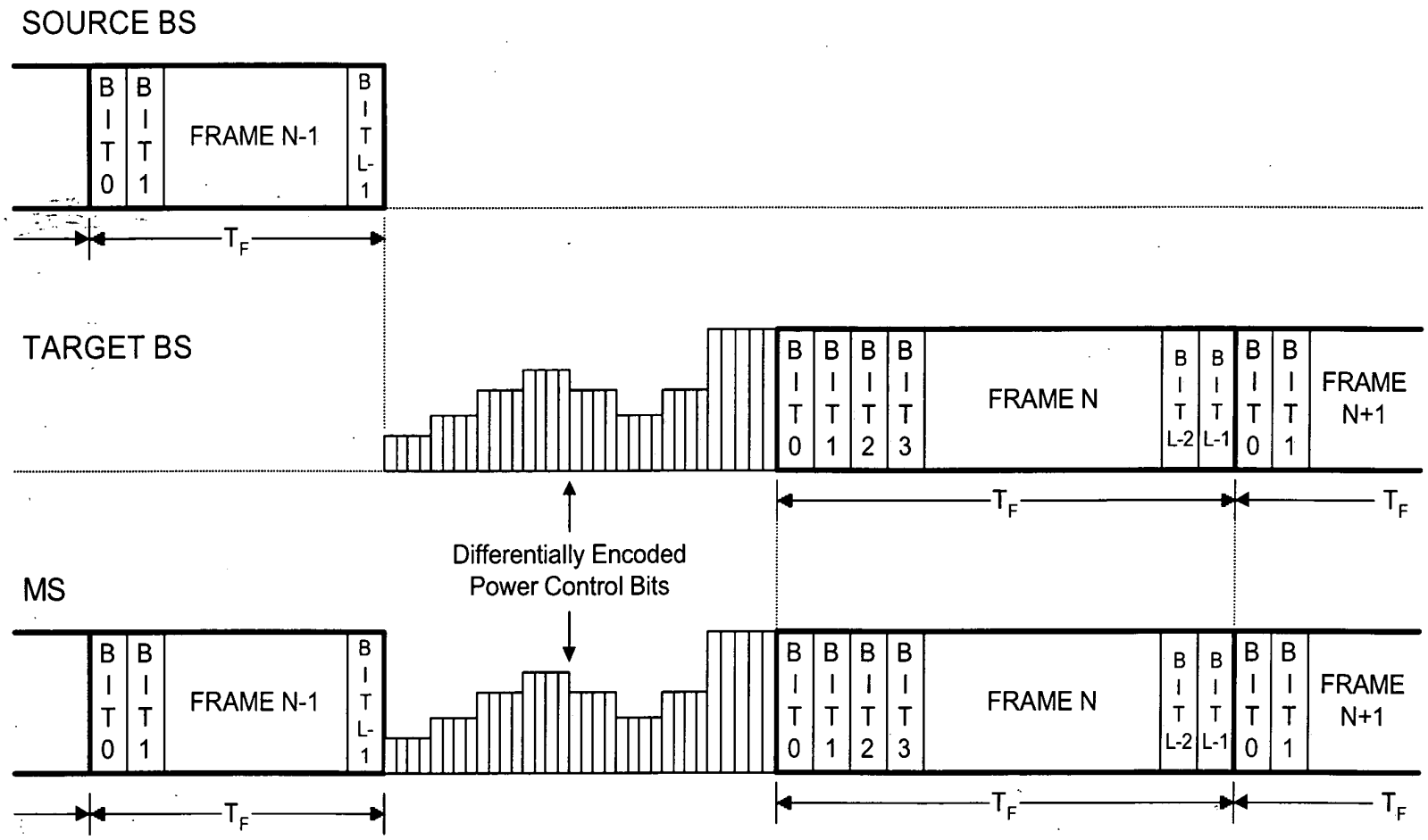
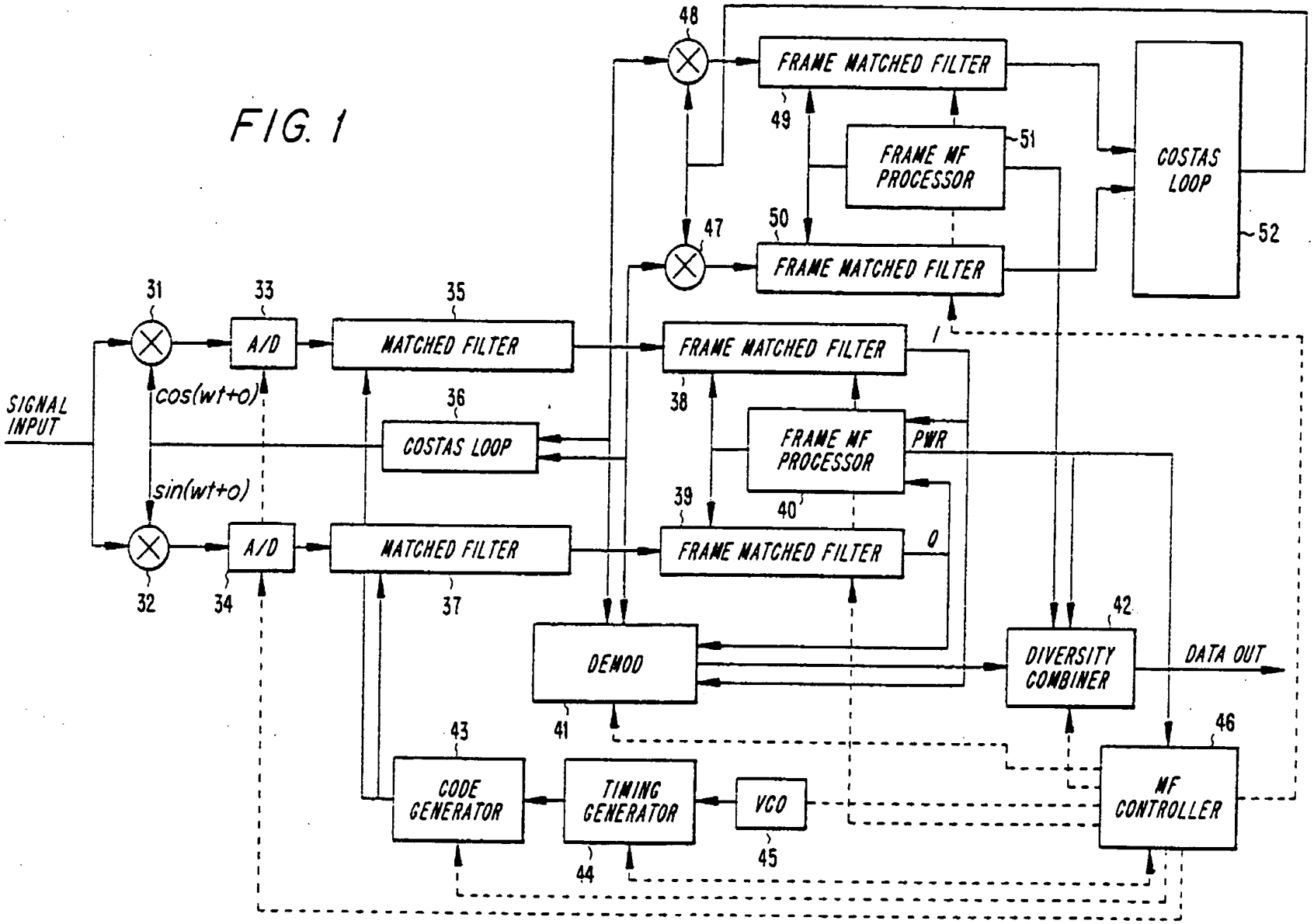

SOURCE BS
BIT 0
BIT 1
FRAME N-1
BIT L-1
T_F
TARGET BS
BIT 0
BIT 1
BIT 2
BIT 3
FRAME N
BIT L-2
BIT L-1
BIT 0
BIT 1
FRAME N+1
T_F
T_F
Differentially Encoded
Power Control Bits
MS
BIT 0
BIT 1
FRAME N-1
BIT L-1
BIT 0
BIT 1
BIT 2
BIT 3
FRAME N
BIT L-2
BIT L-1
BIT 0
BIT 1
FRAME N+1
T_F
T_F
T_F

FIG. 26

FIG. 1



6324207

FIG. 2

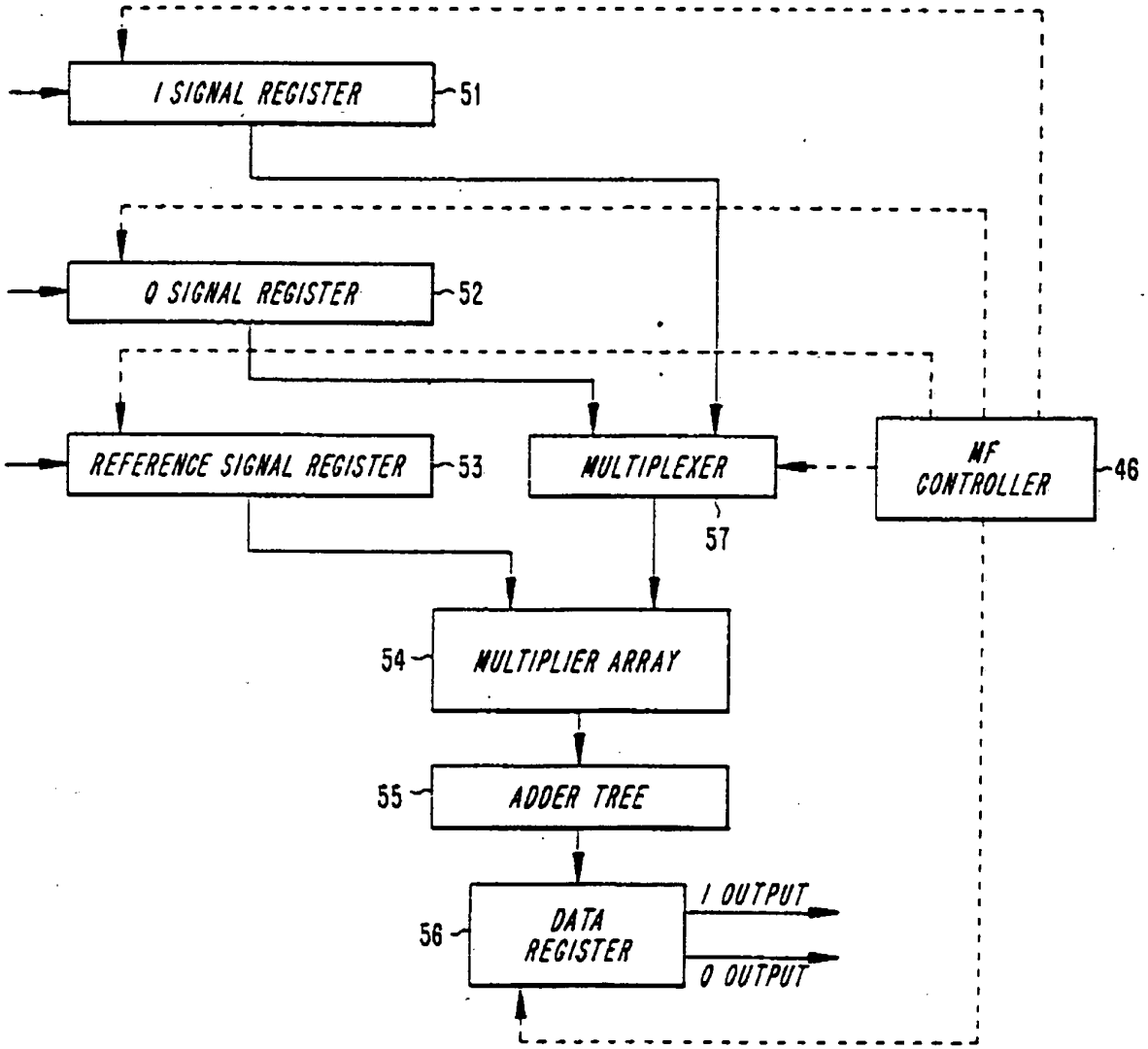

I SIGNAL REGISTER
51
Q SIGNAL REGISTER
52
REFERENCE SIGNAL REGISTER
53
MULTIPLEXER
57
MF CONTROLLER
46
54
MULTIPLIER ARRAY
55
ADDER TREE
56
DATA REGISTER
I OUTPUT
Q OUTPUT

FIG. 3

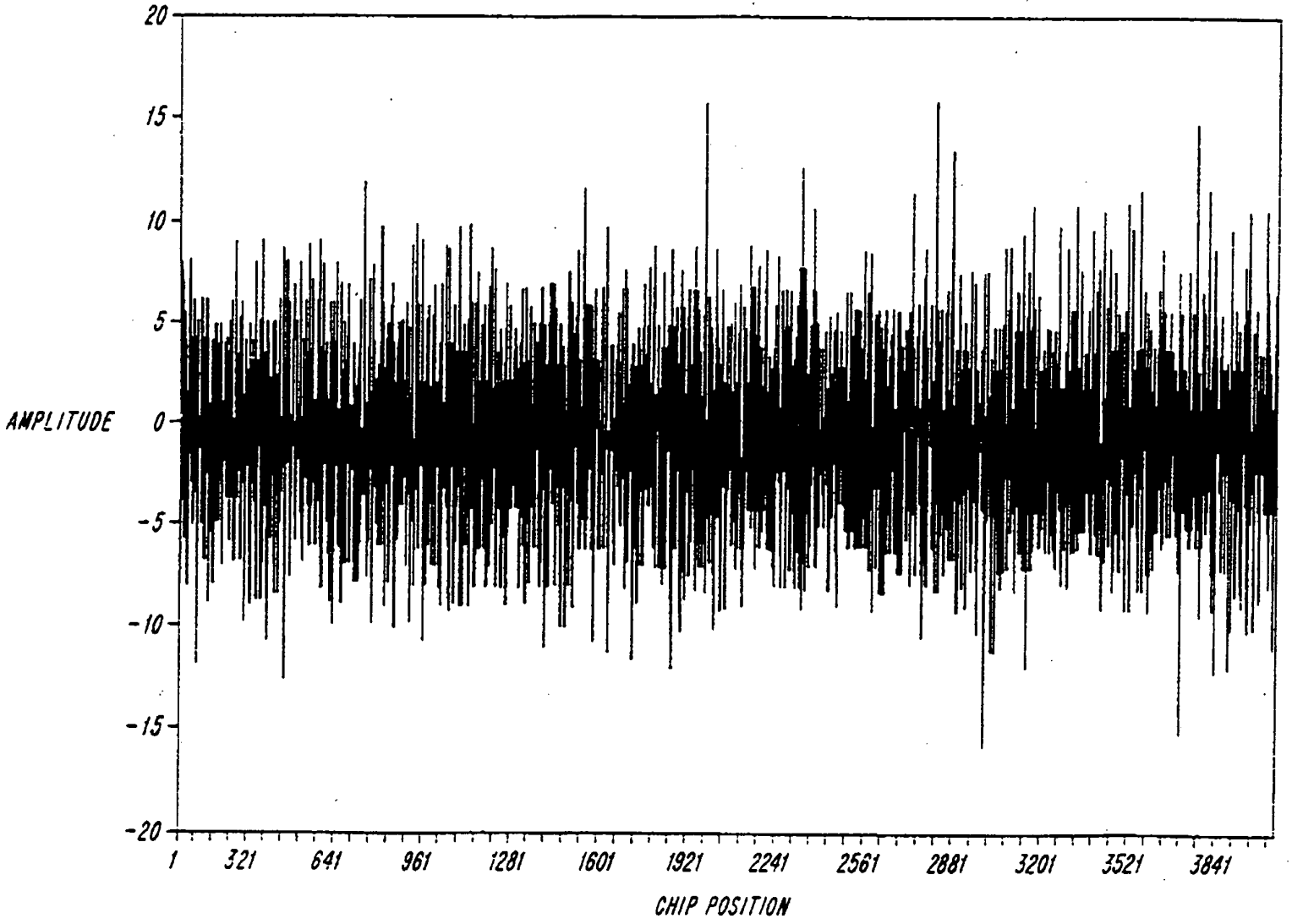

20
15
10
5
0
-5
-10
-15
-20
AMPLITUDE
1
321
641
961
1281
1601
1921
2241
2561
2881
3201
3521
3841
CHIP POSITION

FIG. 4

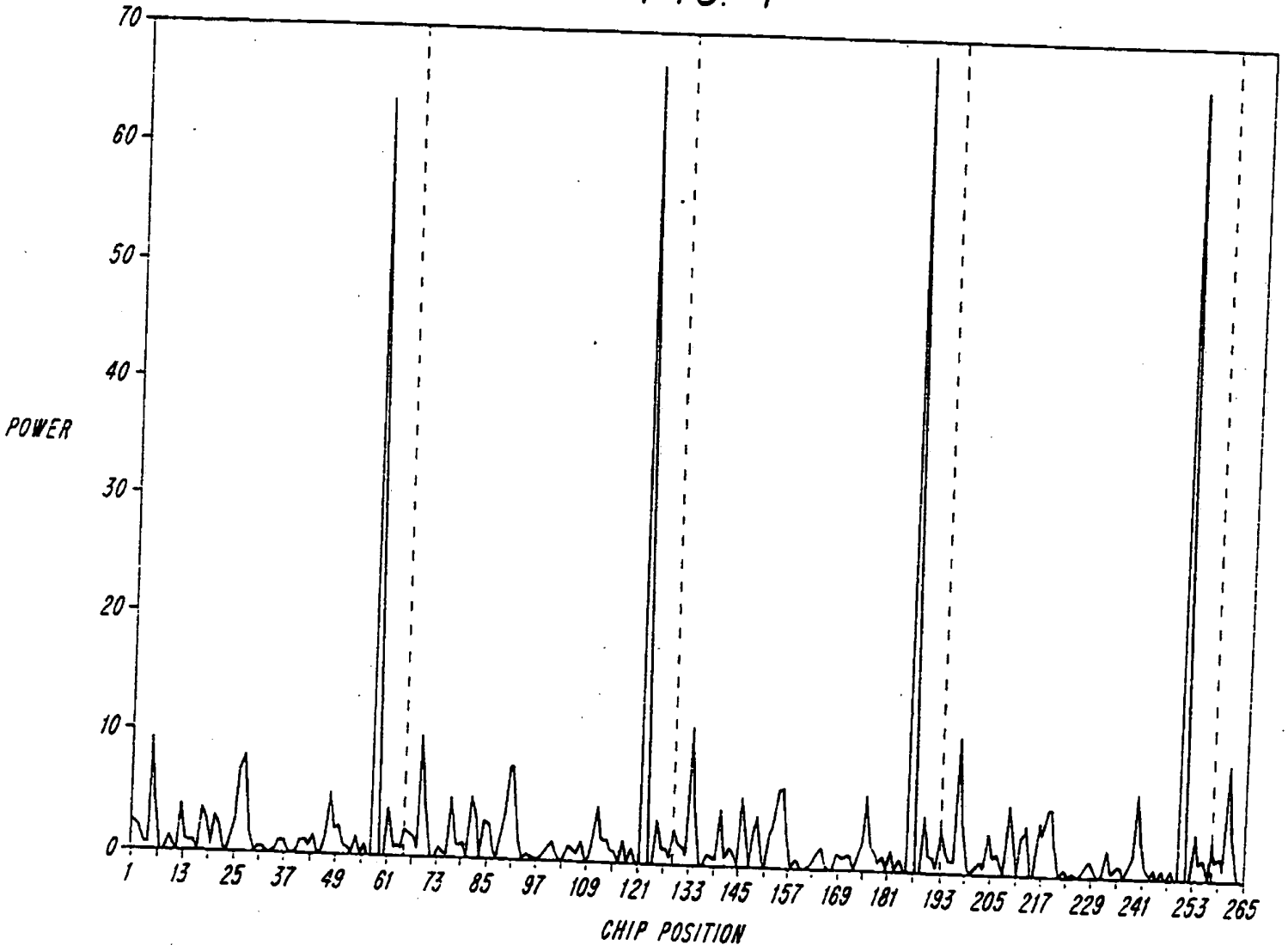

70
60
50
40
30
20
10
0
POWER
1
13
25
37
49
61
73
85
97
109
121
133
145
157
169
181
193
205
217
229
241
253
265
CHIP POSITION

FIG. 5

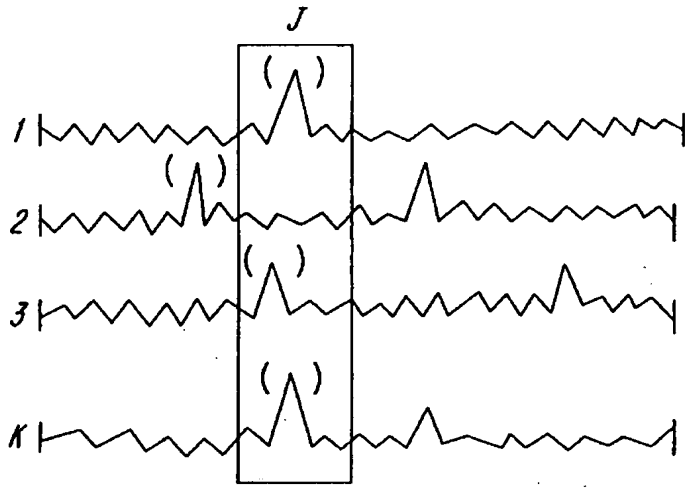


FIG. 6

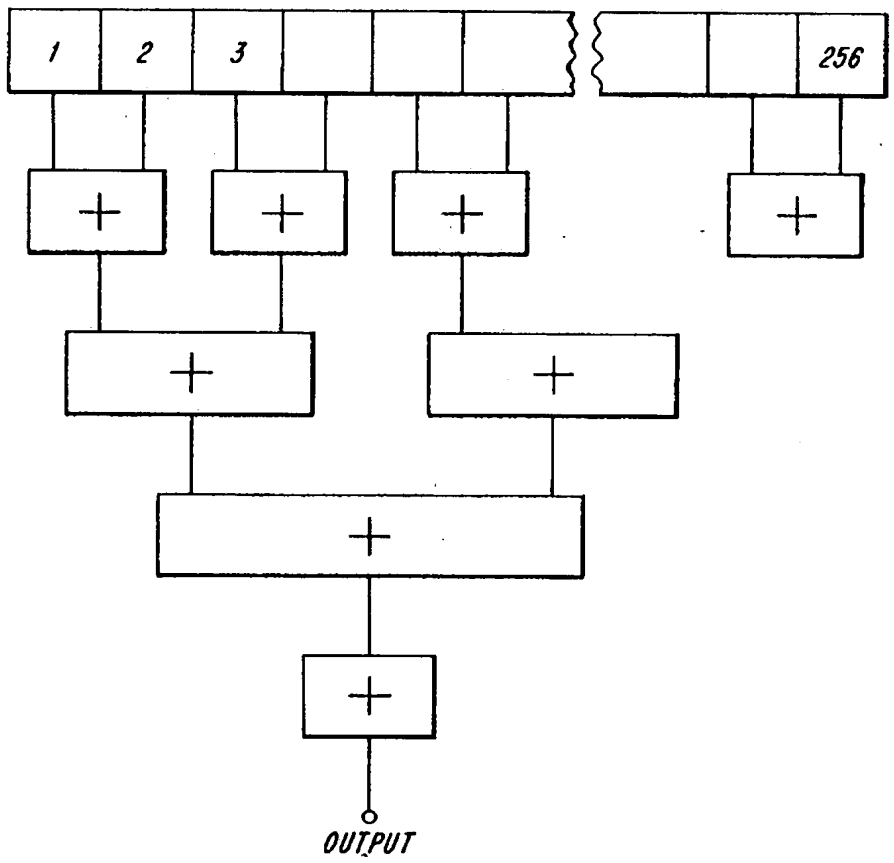


FIG. 7

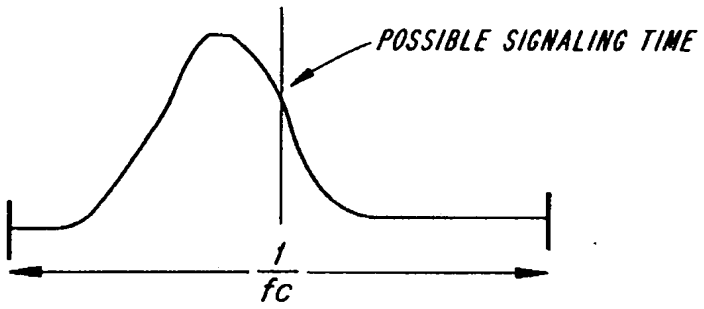


FIG. 8

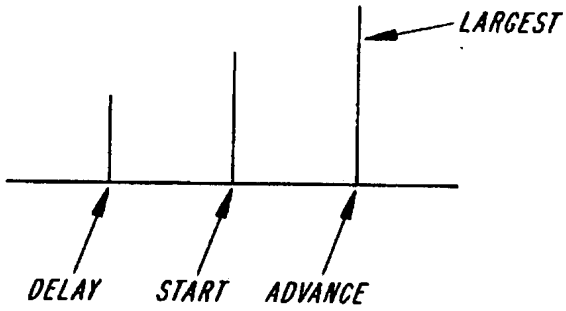


FIG. 9

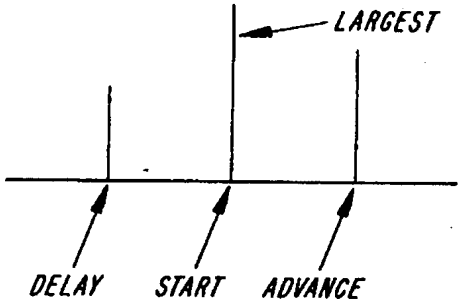


FIG. 10

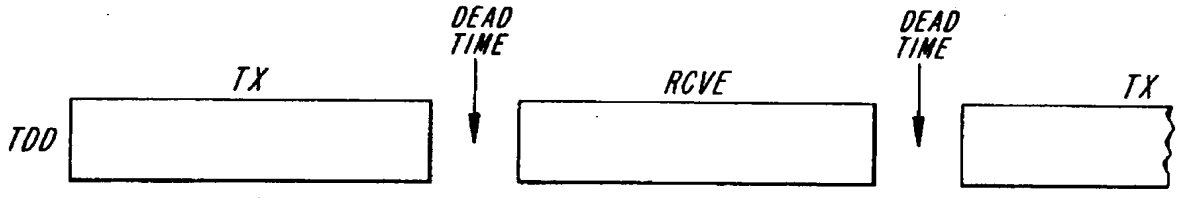


FIG. 11

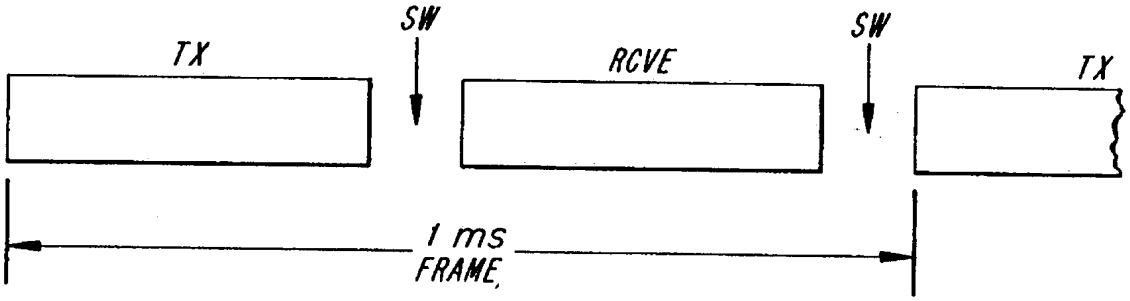


FIG. 12

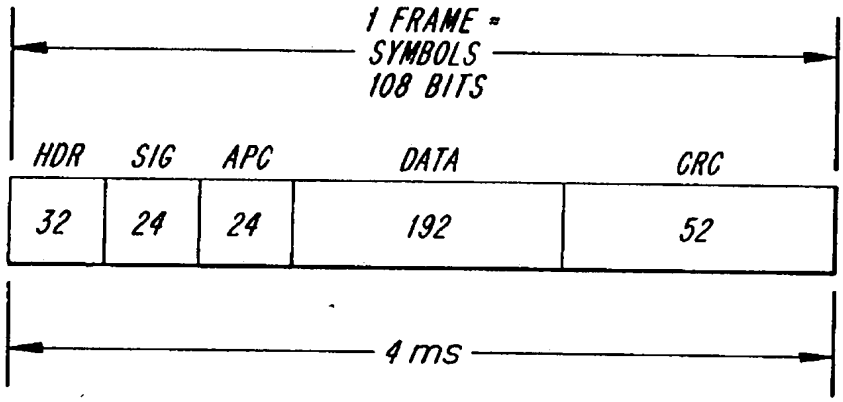
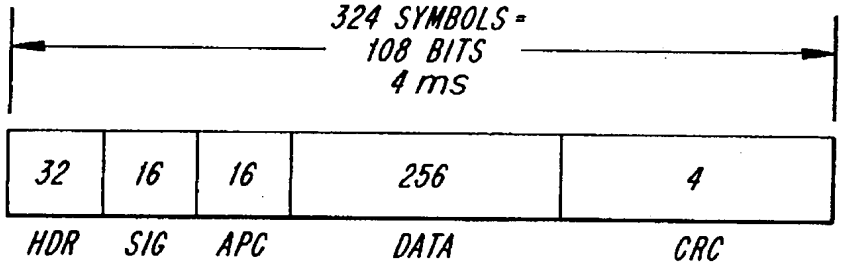


FIG. 13



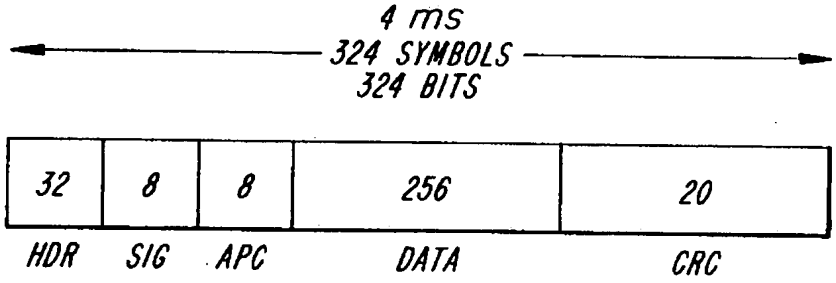


FIG. 14

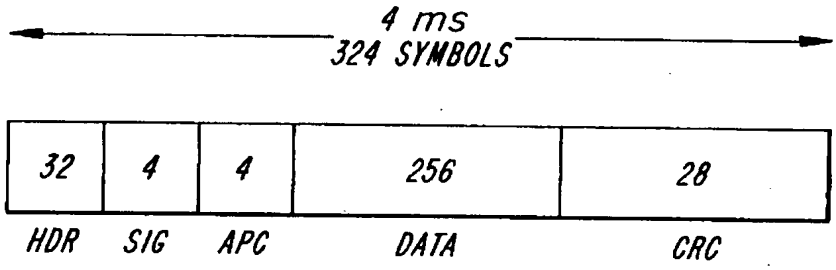


FIG. 15

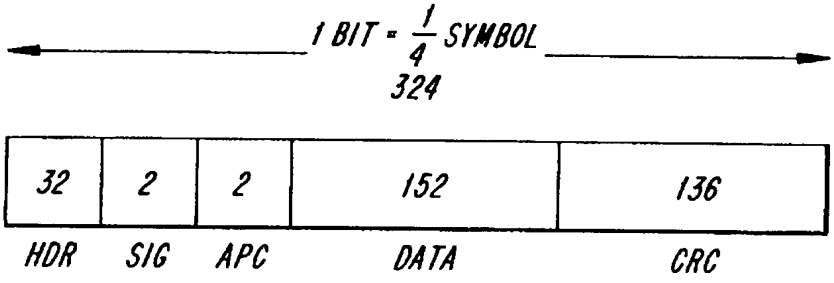


FIG. 16

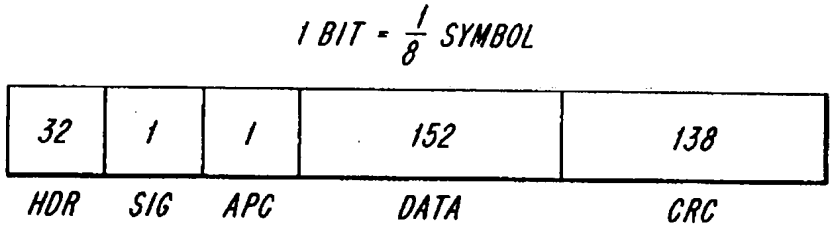


FIG. 17

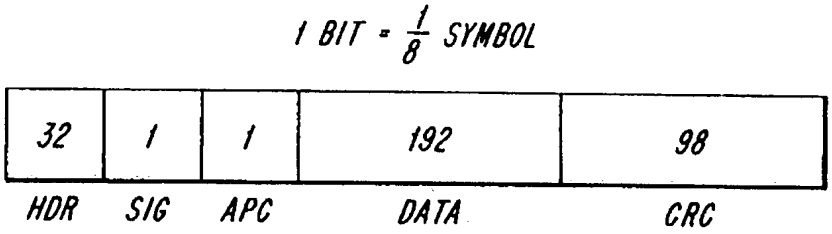


FIG. 18

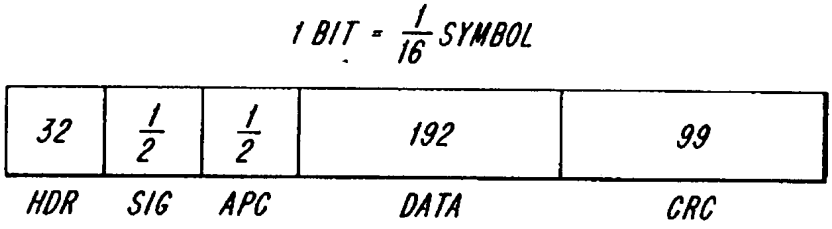


FIG. 19

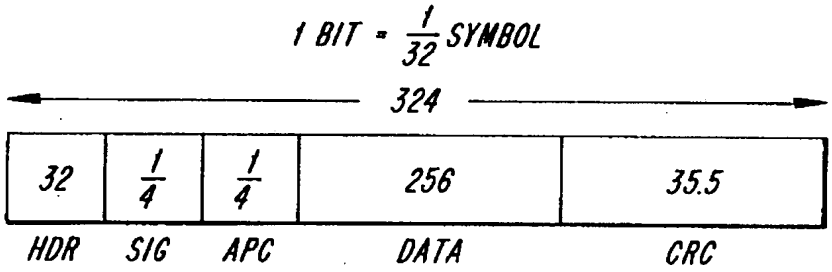


FIG. 20

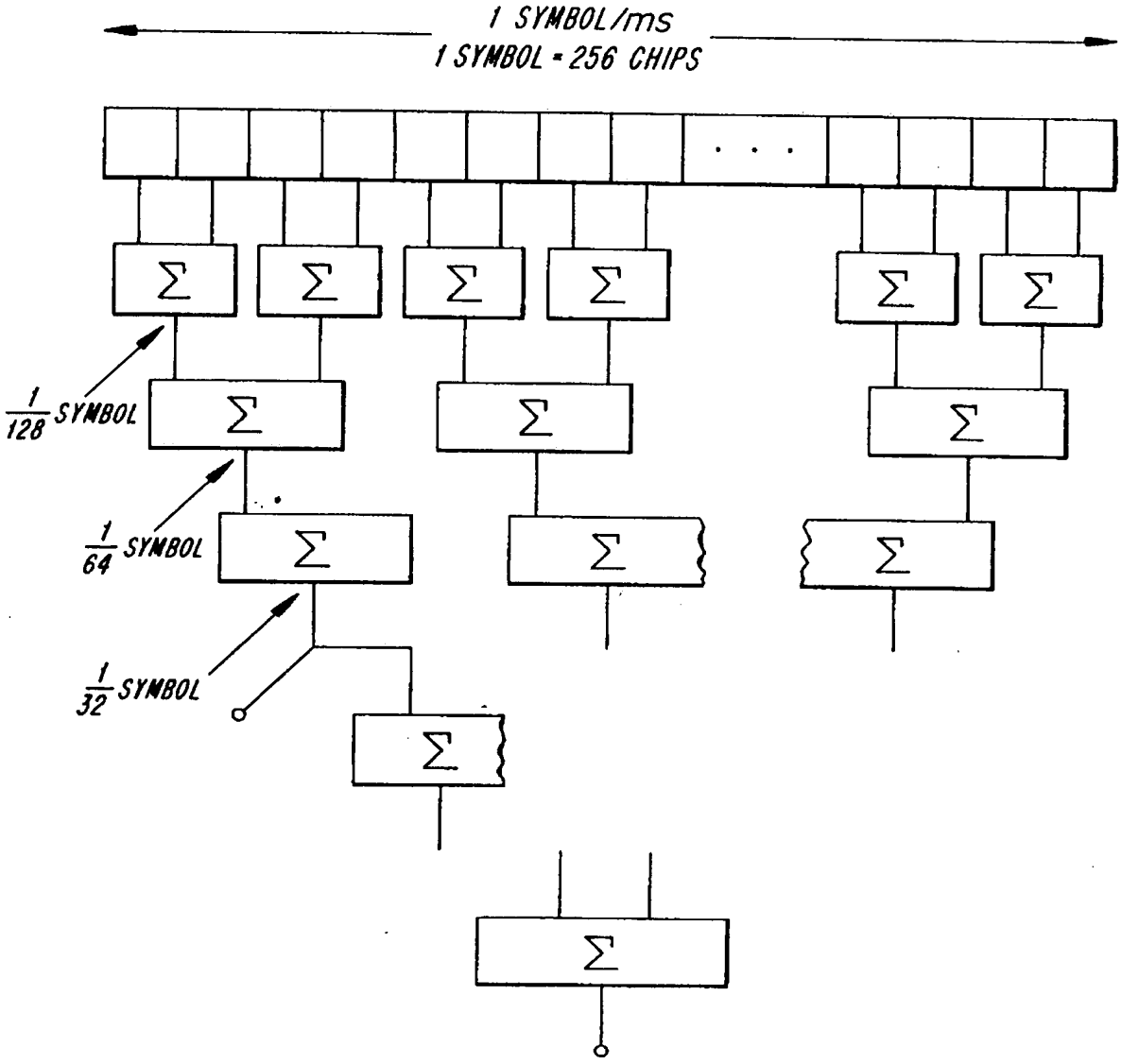

1 SYMBOL/ms
1 SYMBOL = 256 CHIPS
1/128 SYMBOL
1/64 SYMBOL
1/32 SYMBOL
Σ

FIG. 21

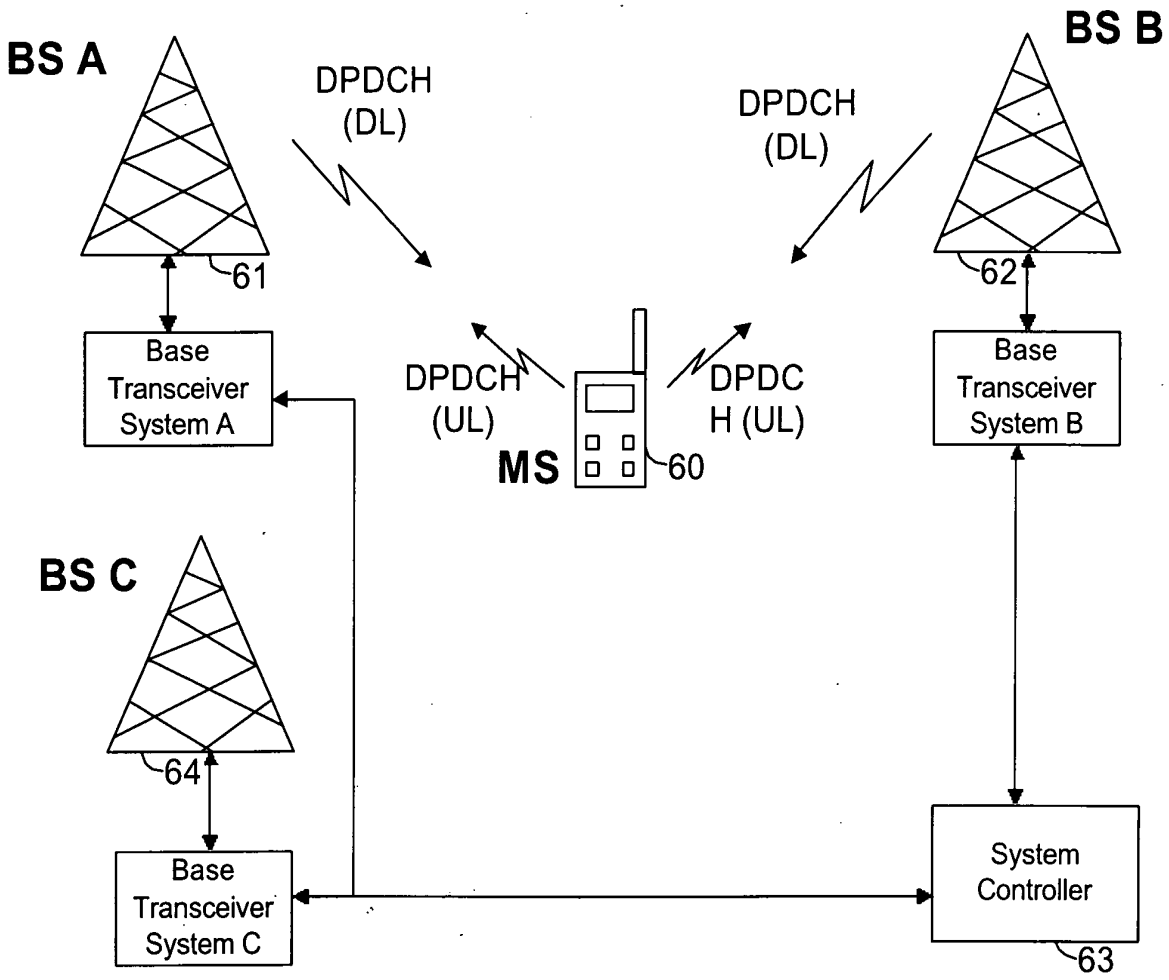

BS A
DPDCH
(DL)
DPDCH
(DL)
BS B
61
62
Base
Transceiver
System A
DPDCH
(UL)
MS
60
DPDC
H (UL)
Base
Transceiver
System B
BS C
64
Base
Transceiver
System C
System
Controller
63

FIG. 22

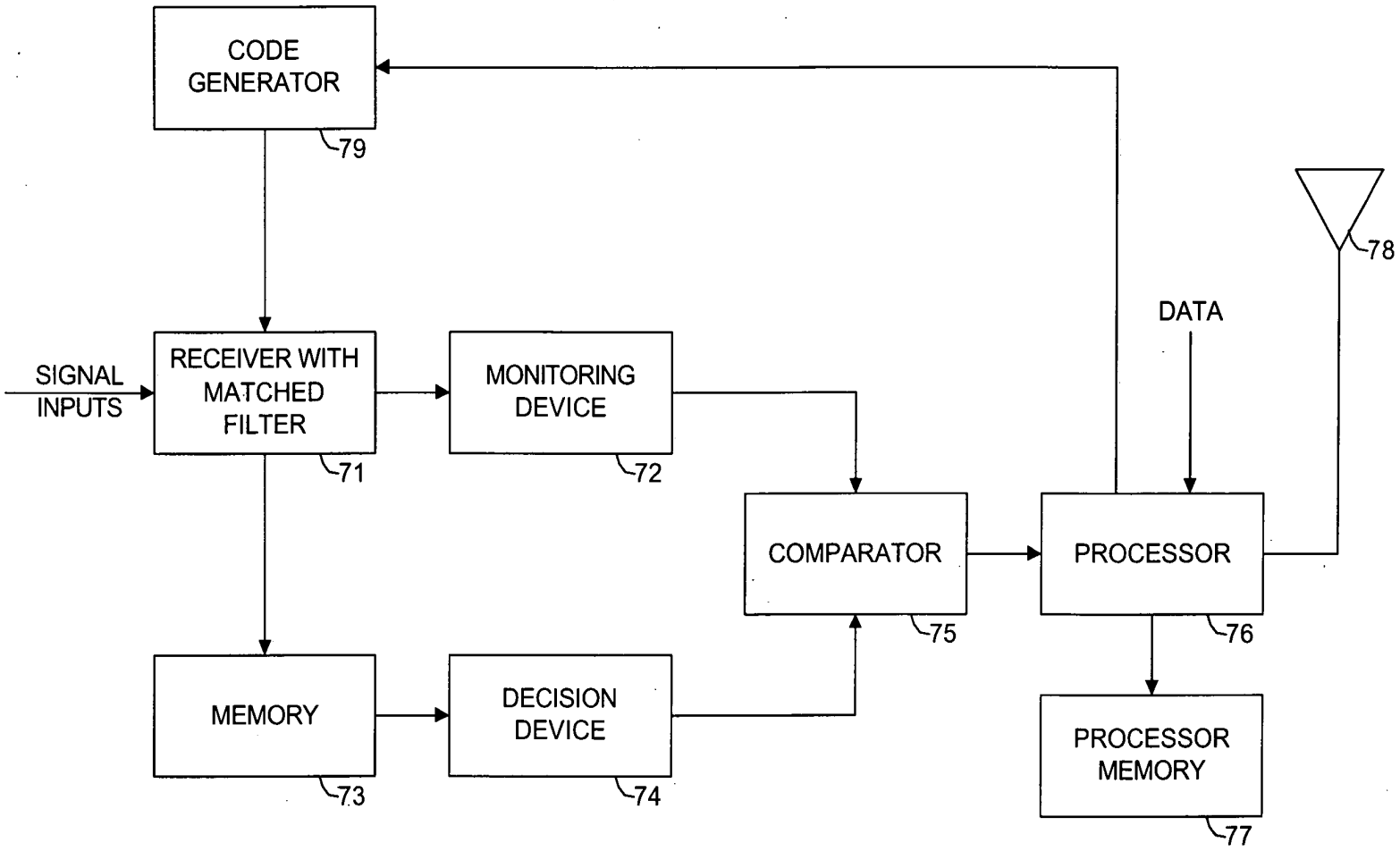

CODE GENERATOR
79
78
DATA
SIGNAL INPUTS
RECEIVER WITH MATCHED FILTER
71
MONITORING DEVICE
72
COMPARATOR
75
PROCESSOR
76
MEMORY
73
DECISION DEVICE
74
PROCESSOR MEMORY
77

FIG. 23

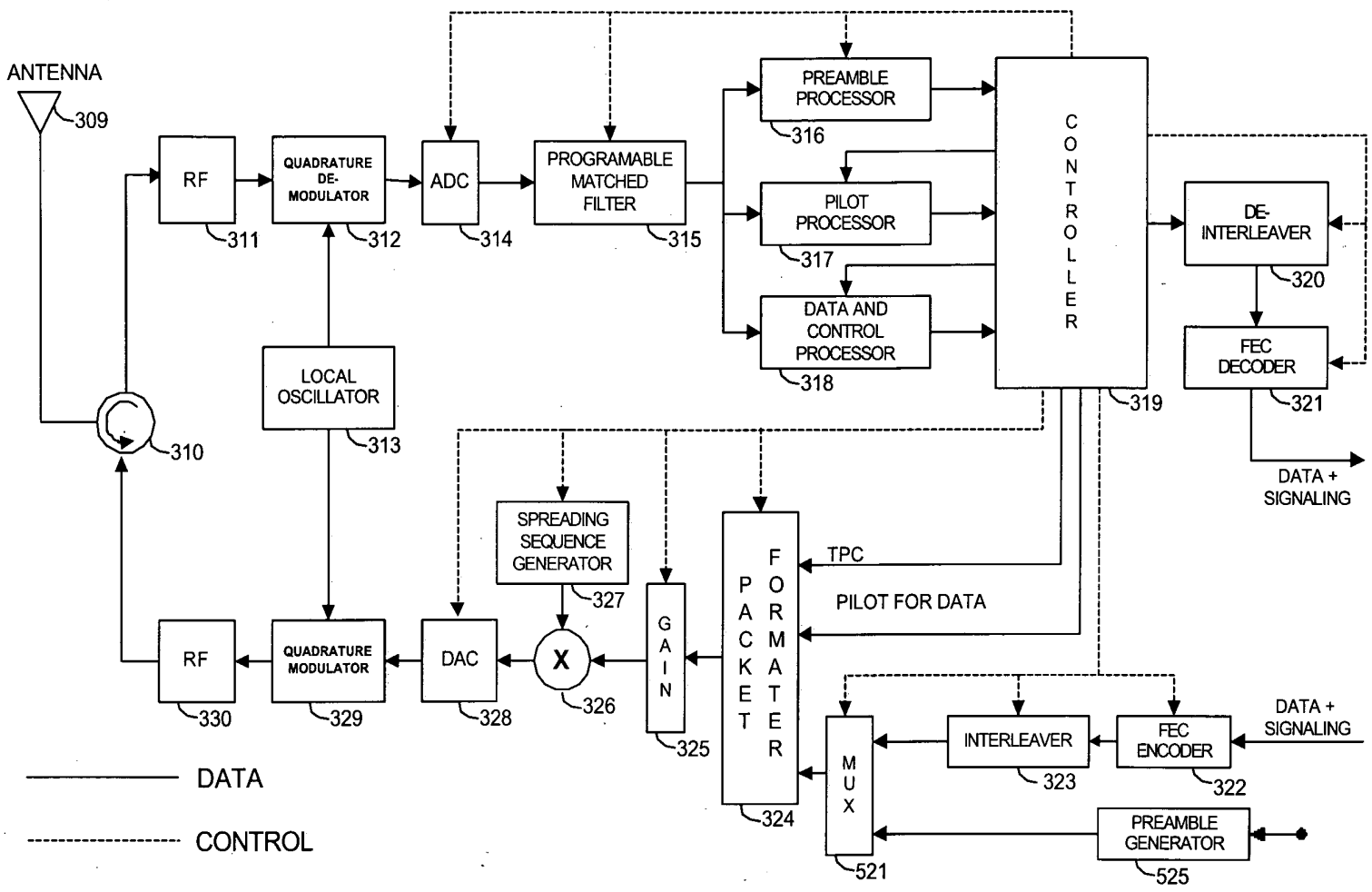

ANTENNA
309
RF
311
QUADRATURE DE-MODULATOR
312
ADC
314
PROGRAMABLE MATCHED FILTER
315
PREAMBLE PROCESSOR
316
PILOT PROCESSOR
317
DATA AND CONTROL PROCESSOR
318
CONTROLLER
319
DE-INTERLEAVER
320
FEC DECODER
321
DATA + SIGNALING
LOCAL OSCILLATOR
313
310
SPREADING SEQUENCE GENERATOR
327
TPC
PILOT FOR DATA
PACKET FORMATER
324
GAIN
325
X
326
RF
330
QUADRATURE MODULATOR
329
DAC
328
MUX
521
INTERLEAVER
323
FEC ENCODER
322
DATA + SIGNALING
PREAMBLE GENERATOR
525
DATA
CONTROL

FIG. 24